ABSTRACT OF THE DISCLOSURE

A semiconductor data processor has a first memory(6) constituting a cache memory, a second memory(20) capable of being a cacheable area or a non-cacheable area by the first memory, and a read buffer(12) capable of carrying out an operation for outputting data corresponding to a read access when the second memory is read accessed as the non-cacheable area. The designation of the cacheable area and the non-cacheable area for the second memory is determined by the designation of a cacheable area or a non-cacheable area for a memory space to which the second memory is mapped. The designation may be carried out in the operation mode of the data processor or by setting a control register, for example.